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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,193	11/26/2003	Byeong-chan Lee	5649-1225	6744

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EV

Office Action Summary	Application No.	Applicant(s)	
	10/722,193	LEE ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,19-24 and 27* is/are rejected.

7)☒ Claim(s) *17,18,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6 and 9-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada et al. (US/6,906,384).

Re claim 1,Yamada et al. disclose an integrated circuit device comprising: a gate electrode (16d, 16e 16i, 16j) (see Figs, 1B, 1C, 3A, 4B and 4C respectively) on an active region (i.e., the region between the source and drain as label as SOI) of an integrated circuit device and on a field isolation layer (STI) (see Figs, 1B, 1C, 3A, 4B and 4C respectively) adjacent to the active region (A); a source region and a drain region (14d, 15d ; 14e, 15e ...) (see Figs, 1B, 1C, 3A, 4B and 4C respectively) in the active region on alternate sides of the gate electrode (16d, 16e 16i, 16j) (see Figs, 1B, 1C, 3A, 4B and 4C respectively); and at least one buried insulation layer (BOX) beneath the drain region or the source region (14d, 15d ; 14e, 15e...), wherein a top surface of the buried insulation layer (BOX) is higher than a bottom surface of the field isolation layer (STI) (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 2, as applied to claim 1 above, Yamada et al. disclose all the claimed limitations including a channel silicon layer (not labeled) covering the buried insulation layer ,

(BOX) in the active region, wherein the source/drain regions are disposed in the channel silicon layer (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 3, as applied to claim 2 above, Yamada et al. disclose all the claimed limitations including wherein the channel silicon layer comprises epitaxially grown single crystalline silicon (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 4, as applied to claim 1 above, Yamada et al. disclose all the claimed limitations including wherein the gate electrodes cross topsides of the active region (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 5, as applied to claim 4 above, Yamada et al. disclose all the claimed limitations including wherein the top levels of the field isolation layers are lower than top surfaces of the active regions (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 6, as applied to claim 4 above, Yamada et al. disclose all the claimed limitations including wherein the gate electrodes fill grooves at boundaries between the active regions and the field isolation layers that expose top sides of the active regions (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 9, as applied to claim 1 above, Yamada et al. disclose all the claimed limitations including wherein the buried insulation layer and the field isolation layers comprise the same material (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 10, as applied to claim 1 above, Yamada et al. disclose all the claimed limitations including wherein the buried insulation layer contacts a bottom surface of the drain region (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 11, as applied to claim 1 above, Yamada et al. disclose all the claimed limitations including wherein the buried insulation layer includes at least one vacancy (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 12, Yamada et al. disclose a method of fabricating an integrated circuit device, comprising: forming a gate electrode on an active region of substrate and on a field isolation layer adjacent to the active region; forming a source region and a drain region (S/D) in the active region on alternate sides of the gate electrode; and forming at least one buried insulation layer beneath the source region or the drain region, wherein a top surface of the buried insulation layer (BOX) is higher than a bottom surface of the field isolation layer (STI) (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Re claim 13, as applied to claim 12 above, Yamada et al. all the claimed limitations including a channel silicon layer between the source/drain regions and above the buried insulation layer (see Figs. 1B-4C and related text Col. 4, line 39 – Col. 8, line 49).

Claims 14, 16, 19-24 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Hieda et al. (US/6,482,714).

Re claim 14, Hieda et al. disclose a method of fabricating an integrated circuit device, comprising: forming at least one passivation layer (103) in a predetermined region of an integrated circuit substrate (101); forming a channel silicon layer (102) on the substrate (101) and the passivation layer (103); patterning the channel silicon layer and the substrate to expose sides of the passivation layer and to forming a trench defining an active region (see Fig. 4B); selectively removing the exposed passivation layer to form a vacant space; and forming a buried

insulation layer in the vacant space and forming a field isolation layer in the trench (see Figs. 4B, 6B, 8B).

Re claim 16, as applied to claim 14 above, Hieda et al. disclose all the claimed limitations including the limitation wherein the passivation layer comprises a material having an etch selectivity relative to the substrate and the channel silicon layer (see Figs. 4B, 6B, 8B).

Re claim 19, as applied to claim 14 above, Hieda et al. disclose all the claimed limitations including the limitation wherein forming a buried insulation layer and a field isolation layer comprises: depositing the field isolation layer to fill the vacant space and the trench; and planarizing the field isolation layer, wherein a portion of the field isolation layer fills the vacant space to form the buried insulation layer (see Figs. 4B, 6B, 8B).

Re claim 20, as applied to claim 19 above, Hieda et al. disclose all the claimed limitations including the limitation forming a thermal oxide layer in the vacant space and the trench prior to depositing the field isolation layer, wherein the thermal oxide layer in the vacant space and the field isolation layer form the buried insulation layer and the thermal oxide layer in the trench forms a sidewall oxide layer (see Figs. 4B, 6B, 8B).

Re claim 21, as applied to claim 14 above, Hieda et al. disclose all the claimed limitations including the limitation wherein forming a buried insulation layer and the field isolation layer comprises: forming the buried insulation layer to fill the vacant space; depositing the field isolation layer to fill the trench; and planarizing the field isolation layer to within the trench, wherein the buried insulation layer comprises a thermal oxide (see Figs. 4B, 6B, 8B).

Re claim 22, as applied to claim 21 above, Hieda et al. disclose all the claimed limitations including the limitation wherein forming the buried insulation layer comprises

thermally oxidizing the substrate containing the vacant space and the trench to form the buried insulation layer filling the vacant space and a sidewall oxide layer in the trench.

Re claim 23, as applied to claim 14 above, Hieda et al. disclose all the claimed limitations including the limitation performing the following steps after forming the buried insulation layer and the field isolation layer: forming a gate electrode on the active region and the field isolation layer; and forming impurity diffusion layers in the active regions on both sides of the gate electrode to provide a source and a. drain region, wherein at least one of the source and drain regions is on the buried insulation layer (see Figs. 4B, 6B, 8B).

Re claim 24, as applied to claim 23 above, Hieda et al. disclose all the claimed limitations including the limitation performing the following steps before forming the gate electrode: recessing the field isolation layer to expose top sides of the active region, wherein the gate electrode crosses top and sides of the active region (see Figs. 4B, 6B, 8B).

Re claim 27, as applied to claim 14 above, Hieda et al. disclose all the claimed limitations including the limitation wherein the buried insulation layer includes at least one vacancy therein (see Figs. 4B, 6B, 8B).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US/6,906,384), as applied in Paragraph 2 above, in view of Hieda et al. (US/6,482,714).

Re claim 7, as applied in claim 6 in Paragraph 2 above, Yamada et al. disclose all the claimed limitations.

However, Yamada et al. do not specifically disclose a recessed liner layer beneath the field isolation layer, wherein inner sides of the grooves include sides of the active regions and the top sides of the field isolation layers adjacent to the top sides of the active regions and the bottom of the grooves defined by the recessed liner layers.

Hieda et al. disclose a recessed liner layer (104) beneath the field isolation layer (105), wherein inner sides of the grooves include sides of the active regions and the top sides of the field isolation layers adjacent to the top sides of the active regions and the bottom of the grooves defined by the recessed liner layers (104) (see Figs. 2B, 9B and 11-18A).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Yamada et al. reference with a recessed liner layer beneath the field isolation layer, wherein inner sides of the grooves include sides of the active regions and the top sides of the field isolation layers adjacent to the top sides of the

active regions and the bottom of the grooves defined by the recessed liner layer as taught by Hieda et al. in order to provide passivation of the shallow trench isolation region.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US/6,906,384).

Re claim 8, as applied in claim 1 in Paragraph 2 above, Yamada et al. disclose all the claimed limitations including the buried oxide insulation comprises oxide layer. However, it within the scope Yamada et al. disclosure that the oxide layer can be thermal oxide layer because it is well-known in the art to provide a thermal oxide as buried insulation layer due to its high quality. Therefore, Examiner takes an Official notice because it is well-known in the art to provide a thermal oxide layer as buried oxide layer due its high quality. See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942). See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda et al. (US/6,482,714).

Re claim 15, as applied to claim 14 in Paragraph 4, Hieda et al. disclose all the claimed limitations including the limitation wherein the passivation layer and the channel silicon layer formed by well-known deposition process. In addition formation of the layer by ultra-high vacuum chemical vapor deposition or low-pressure chemical vapor deposition is within the scope of Hieda et al. because these process are routinely used to from films silicon, silicon oxide silicon nitride and others due to low thermal budget and to maintain high quality of the deposited film. Therefore, Examiner takes an Official notice because it is well-known in the art formation of the layer by ultra-high vacuum chemical vapor deposition or low-pressure chemical vapor

deposition is within the scope of Hieda et al. because these process are routinely used to from films silicon, silicon oxide silicon nitride and others due to low thermal budget and to maintain high quality of the deposited film. See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942). See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Allowable Subject Matter

8. Claims 17, 18, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicants' arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on September 30, 2005.

10. Applicants' arguments filed on September 30, 2005 with respect to claims 14-16 and 19-24 have been fully considered but they are not persuasive.

With respect claims 14-16 and 19-24, applicants argue that "Hieda does not teach forming a channel silicon layer on the substrate and on the passivation layer ..."

In response to applicant' argument, it is respectfully submitted that Hieda et al. '714 disclose forming of the channel silicon layer 102 on the passivation layer 103 which passivation layer formed on the substrate 101 thereof as shown in Figs. 4B and 8B.

Therefore, the rejection of claims 14, 16, 19-24 and 27 under 35 U.S.C. § 102 is deemed proper. In addition, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 also deemed proper.

Conclusion

11. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
December 11, 2005